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**REMARKS**

Claim 50 is amended. Claims 50-51 and 71-75 are pending in the application.

Independent claim 50 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Verhaar, U.S. Patent No. 5,015,598 and Park, U.S. Patent No. 5,545,578 in further view of either Hiroki, U.S. Patent No. 5,512,771 or Kurimoto, U.S. Patent No. 5,306,655. The Examiner is reminded by direction to MPEP § 2143 that a proper obviousness rejection has the following three requirements: 1) there must be some suggestion or motivation to modify or combine reference teachings; 2) there must be a reasonable expectation of success; and 3) the combined references must teach or suggest all of the claim limitations. Independent claim 50 is allowable over the cited combinations of Verhaar, Park, Hiroki and Kurimoto for at least the reason that the references, individually or as combined, fail to disclose or suggest each and every element in the claim.

As amended independent claim 50 recites forming a conductive gate structure over the dielectric layer where the gate structure comprises a polysilicon material layer, a conductive reaction barrier layer over the polysilicon layer, a metal layer over the conductive reaction barrier layer and an insulative cap, and where the gate structure has sidewalls which define a lateral dimension of the gate the sidewalls comprising a polysilicon material surface and a metal comprising surface. Claim 50 additionally recites forming a non-oxide material directly against the sidewalls along an entirety of the polysilicon material surface to form a non-exposed polysilicon material surface, and along the entirety of the metal-comprising surface to form a non-exposed metal-comprising surface. Claim 50 further recites anisotropically etching the non-oxide material to form spacers on the

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sidewalls, where the gate dielectric layer extends laterally outward from the gate structure and spacers and while the spacers are on the sidewall and joining the gate dielectric layer, subjecting the substrate to oxidizing conditions where a portion of the non-exposed polysilicon material surface is oxidized during the subjecting. The amendment to claim 50 is supported by the specification at, for example, page 5, line 21 through page 6, line 4; page 7, line 20 through page 8, line 9; and Figs. 3, 5, 7 and 8.

Verhaar discloses a sidewall spacer 20a along a polycrystalline layer 12 and over a dielectric layer 11 (Fig. 4 and the accompanying text). Applicant notes that at the time of re-oxidation as disclosed by Verhaar, dielectric layer 11 does not extend laterally from sidewall spacer 20a. Further, Verhaar does not disclose or suggest the claim 50 recited conductive reaction barrier layer over the polysilicon material layer or the recited metal layer over the conductive reaction barrier layer. Verhaar additionally fails to disclose or suggest the claim 50 recited oxidation of a non-exposed polysilicon material surface during oxidation of a substrate where spacers protect a metal comprising surface and a portion of the non-exposed polysilicon material surface from oxidation.

Park discloses utilization of spacers which cover less than an entire length of a polysilicon surface to allow oxidation to occur in the exposed area not covered by the spacers (col. 4, ll. 58 through col. 5, ll. 14). Park further discloses that the gate structure comprises a layer of tungsten silicide 16 over the polysilicon material 14. Park does not disclose or suggest the claim 50 recited metal layer over a conductive reaction barrier layer which is disposed over a polysilicon material layer of a gate structure. Applicant notes with reference to applicant's specification at page 6, lines 3-4 that the barrier layer as recited in claim 50 prevents formation of a silicide. Park, however, specifically utilizes a silicide in the

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gate structure. Accordingly, as combined with Verhaar, Park fails to contribute toward suggesting the claim 50 recited conductive gate structure comprising a metal layer over a conductive reaction barrier layer which is disposed over a polysilicon material layer, or the recited portion of the non-exposed polysilicon material layer being oxidized while spacers are on the sidewalls protecting the metal-comprising surface and a portion of non-exposed silicon material surface from oxidation. Accordingly, claim 50 is not rendered obvious by the combination of Verhaar and Park.

As indicated by the Examiner at page 4 of the present Action, Hiroki and Kurimoto are relied upon as teaching formation of a "smiling gate" by oxidizing a portion of a polysilicon material. However, applicant notes in each of these references the relevant polysilicon material which is oxidized is specifically indicated as being covered by an oxide material to allow oxidation of the polysilicon material. Accordingly, neither Kurimoto nor Hiroki contributes towards suggesting oxidizing a portion of a polysilicon surface which is covered by sidewall spacers comprised of non-oxide material. Further, neither Kurimoto nor Huroki contributes toward suggesting the claim 50 recited oxidation of a polysilicon material layer of a gate structure where the gate structure includes a conductive reaction barrier layer over the polysilicon material layer and a metal layer over the conductive reaction barrier layer. Accordingly, independent claim 50 is not rendered obvious by the recited combinations of Verhaar, Park, Hiroki and Kurimoto and is allowable over these references.

Dependent claims 51 and 71-75 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Verhaar, Park and Hiroki or Kurimoto, as further combined with one or more of Pierce, U.S. Patent No. 5,422,289; Iijima, U.S. Patent No.

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5,903,053; Kumagai, U.S. Patent No. 5,430,313 and Brigham, U.S. Patent No. 5,714,413. As indicated at page 5 of the present Action each of Pierce and Iijima are relied upon as disclosing a metal comprising layer in a gate structure. However, neither Pierce nor Iijima discloses or suggests the claim 50 recited metal layer being disposed over a conductive reaction barrier layer which is in turn over a polysilicon material layer. Accordingly, as combined with Verhaar, Park, Hiroki and Kurimoto, neither Pierce nor Iijima contributes toward suggesting the claim 50 recited conductive gate structure comprising a poly material layer, a conductive reaction barrier layer and a metal layer, or the recited subjecting the substrate to oxidizing conditions which oxidizes a non-exposed portion of the polysilicon material layer while non-oxide spacers are present on the sidewalls and joining the gate dielectric layer during the oxidation.

As indicated at page 8 of the present Action, Kumagai and Brigham are relied upon as showing formation of various double sidewall spacers. However, the various sidewall spacers disclosed by Kumagai and Brigham do not contribute toward suggesting the claim 50 recited substrate having a conductive gate structure comprising a metal layer over a conductive reaction barrier layer which is disposed over a polysilicon material layer. Nor do these references contribute to the recited oxidizing a portion of a non-exposed polysilicon material surface which is covered by a non-oxide sidewall spacer which joins with the gate dielectric layer. Accordingly, independent claim 50 is not rendered obvious by the various cited combinations of Verhaar, Park, Hiroki, Kurimoto, Pierce, Iijima, Kumagai and Brigham and is allowable over these references.

Dependent claims 51 and 71-75 are allowable over the various combinations of Verhaar, Park, Hiroki, Kurimoto, Pierce, Iijima, Kumagai and Brigham for at least the

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reason that they depend from allowable base claim 50.

For the reasons discussed above claims 50-51 and 71-75 are allowable. Accordingly, applicant respectfully requests formal allowance of such claims in the Examiner's next action.

Respectfully submitted,

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